Programmable Phase Shift Circuit for an Integrated Power-Meter

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***Abstract*—An architecture of the digital phase shift circuit implemented as a Programmable Delay Line (PDL) is presented in this paper. This block represents an important part of the Decimation filter block, for a particular Power-meter integrated circuit. The chosen architecture is very simple for implementation and uses logic blocks such as multiplexers and buffers. The circuit is described and verified using VHDL language and simulator, and is satisfying the needed requirements.**

***Index Terms*—Decimation filter, Programmable Delay Line, Phase shifter.**

I. Introduction

DIGITAL signal processing is an inevitable task in most of contemporary wide-band applications. Digital techniques and technologies have many advantages over the analog ones, and choosing this domain for signal manipulation facilitates the design, implementation and realization, as well as the application of the system at high frequencies.

In digital signal processing, decimation is the process of reducing the sampling rate of a signal [1], [2], [3]. In systems where they are required, determined by a specified application, it is sometimes necessary to attach some other functionality to it. As a part of a large Power-meter SoC project, it was required to implement A/D conversion using a sigma-delta modulation. The system performs energy measurement and power quality monitoring for 3-Phases power supply signal at standard 50Hz frequency [4]. An important part of the A/D converter subsystem was a decimation filter bank that reduces the 16.384MHz input signal into DSP processable signal at 16kHz frequency [5], [6], [7]. This gave the decimation factor of 1024 [8], [9]. Beside the decimation, it was also required to achieve fine tuning of the signal phase. An architecture that performs this functionality was the subject of this research.

In this paper a short overview of the decimation filter will be given in the next section. This basic architecture was upgraded by a digitally controlled phase shift circuit, which is based on a Programmable Delay Lines (PDL). This will be explained in the third section. The circuit is described using VHDL, and the result of such implementation is given thereafter. VHDL simulations validate the system functionality. Results of circuit simulations and conclusions are provided at the end of this paper.

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II. Decimation Filter in Power-Meter IC

The decimation part of the Power-meter SoC is placed between the sigma-delta conversion circuit and the DSP block. To achieve savings in the IC area the 3-phase signal processing was realized by multiplexing and time-sharing the system's resources. It means that the system represent a single-phase solution to the problem, which is properly modified to work at 3 times higher frequency. The same decimation line processes three input signals that correspond to the particular phases of the power supply voltage. Similar solution is applied to measurement of current signals that are present at each of three phases.

Decimation filters perform several important functions. The first is to down-sample and reduce the clock rate. The second is to remove the entire out-of-band signals and noise. In practice decimation is done in multiple stages by cascading several smaller decimation factors, such that the overall decimation factor equals the product of decimation factors of the individual decimation stages. One big advantage of multistage filtering is the power reduction which is enabled by lower sampling rates for subsequent components. The power reduction, along with reduction in number of filter tabs makes a multistage approach more desirable [10].

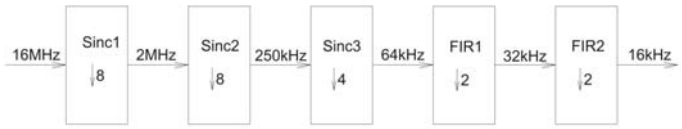

Fig. 1. Basic structure of the decimation line

Each decimation line consists of 5 blocks as shown in Fig. 1. There are three Sinc filters with decimation factor of 8, 8, and 4, and two FIR filters, with decimation factor 2 and 2. The first stage has a heavy impact on the total number of digital filter operations [5], most computational power is concentrated in it. Accordingly, FIR architecture could not be adequate in the first stages of decimation. Sinc filters are chosen as the first three stages since antialiasing requirements are very relaxed, allowing the designer to trade frequency

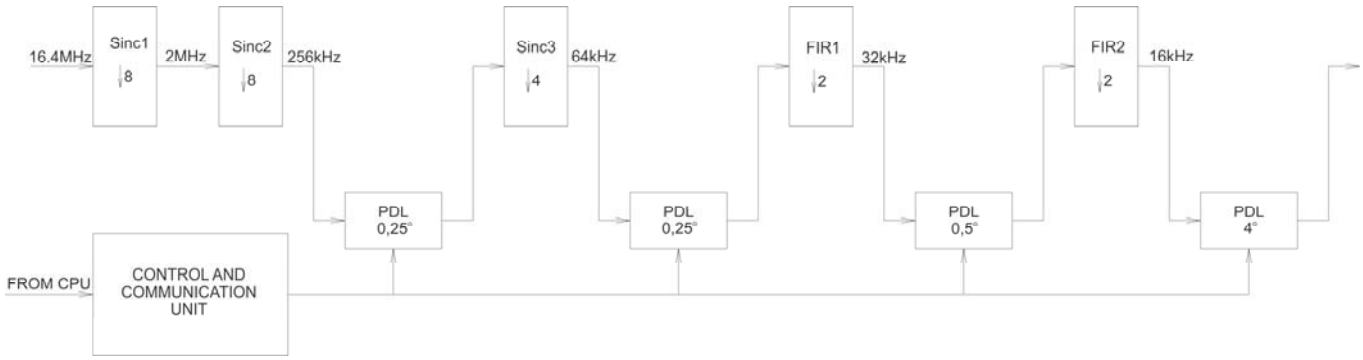

Fig. 2. Decimation filter block with the phase shift control capability

distortion for lower power consumption. This distortion is about to be handled in the following FIR filters. They are based on the CSD (Canonical Signed Digit) representation, and have a hardwired implementation of the chosen coefficients. This realization enables area and power consumption savings as well as high operating frequencies.

Necessary modifications of this basic decimator architecture in order to implement phase shifting control will be explained in detail in the next section.

III. Phase Shifter Realization

The purpose of the PDL line is to postpone or speed up the occurrence of the filtered signal at the output of the decimation line, depending on the input control word.

The requirements for phase control are: the phase shifting range is ±5 degrees, and minimal phase shifting step of 0.25 degrees. Since the phase shifter is a programmable part of the decimator, it is necessary to have a digital word that corresponds to this requirement. It is highly preferable to keep the length of this word as small as possible.

As can be seen from Fig. 1, there are several available clock signals. The decimator operates at 6 different frequencies: 16kHz, 32kHz, 64kHz, 256kHz, 2.048MHz, and 16.384MHz. Lengths of digital words that are obtained at the outputs of corresponding decimation stages are: 12 bits at the output of the first Sinc filter, 24 bits at the output of the second Sinc filter, 32 bits at output of the third Sinc filter, 16 bits at output of the first FIR filter, and finally, 16 bits at the output of the decimation line. These are available "resources" for creating a programmable phase shifter.

As mentioned above, the phase shift must be bidirectional. It means that the first digit in a control word denotes the sign of the shifting. After many calculation trials, the requirements for minimal length of the control word were met using an 8-bit word.

The choice of signals to delay must also be properly made. If the part of delay line operates with signal that is too fast, some timing and glitch problems may occur. Otherwise, slower signals from the decimation filter line have many bits to handle, since this filter constantly needs to accumulate samples. In this case, too large area of the digital block must be dedicated for this part of delay lines. Nevertheless, it should be mentioned that the output signal of the decimator must not exceed 16 bits due to design specifications.

As can be seen from Fig. 2, first 3 digits of the control word (beginning with LSB representation) can control up to ±4 degrees of phase shift. They are controlled by the slowest clock from the decimation filter that is 16kHz. The following bit can control ±0.5 degrees of the phase shift, and its clock has the frequency of 32kHz. The next bit of the control word can make a phase shift of ±0.25 degrees, while its clock frequency is 64kHz. Two bits determine the phase shift resolution, since the frequency of this part of the delay line is 256kHz. These two bits of the control line can give up to 2x0.125 degrees for the sinusoidal signal at 50Hz. The last bit of the control word is a sign bit. According to available clock frequencies, these values cannot be achieved with 100% accuracy. Instead, some values that are very near the required ones are supported.

IV. VLSI Implementation

The entire architecture of this part of the decimation filter line consists of several basic building blocks. Depending on their place in the line, these building blocks only need to be adjusted according to their particular operating frequency, as well as to the required length of the digital signal at the particular place of the decimator.

Basic configuration of a delay cell is shown in Fig 3. It consists of a shift register, made of D flip-flop, and a demultiplexer.

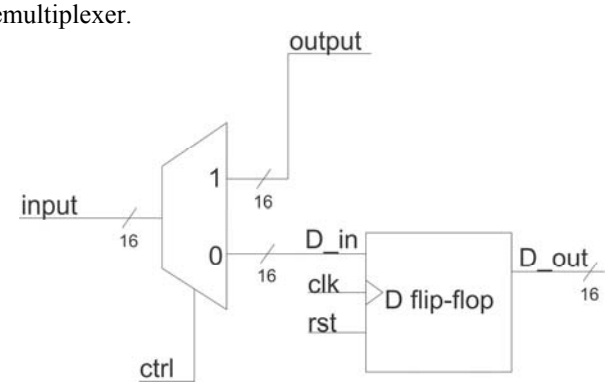

Fig. 3. Delay cell

One additional decoder is needed to resolve the address to the delay cells switching conversion.

All these blocks were described in VHDL, and linked to the basic decimator circuit within a VHDL block-diagram

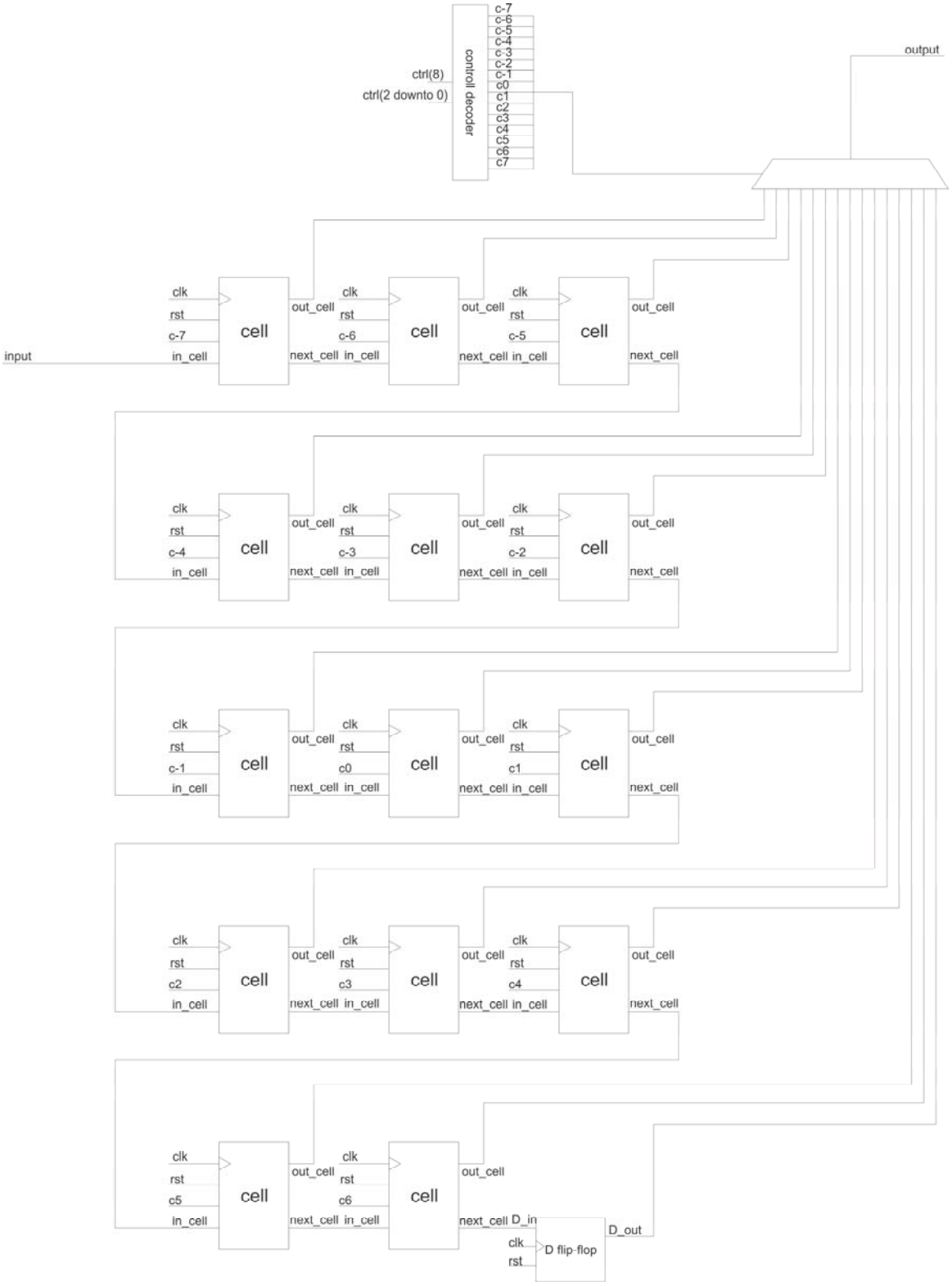

Fig. 4. Part of the programmable delay line, controlled by two bits.

environment. One particular delay block that is connected between second FIR and output of the entire decimation filter is shown in Fig. 4.

Other PDL blocks have different lengths. In order to reuse the same blocks in further descriptions and implementations, lengths of the input and output digital words were described as a VHDL generic.

To verify the correctness of these descriptions, one has to perform many simulations. This will be the subject of the section that follows.

V. Simulation Results

All parts of the PDL line that were described in VHDL were verified in Active HDL simulator. A test bench was written using mostly test bench and results from the decimator filter verification. Additional signals had to be defined in order to check for the controlling capabilities of the PDL.

In order to achieve positive and negative phase shifts, signals that are loaded into PDL blocks are initially delayed for maximum amount of delay. It means that the reference signal at the output of the Sinc2 block is postponed for corresponding 5^o of the maximal phase shift. Signals at Fig. 5, are: *y* - the output signal of the Sinc1 block, *z* - the output signal of the Sinc2 block, *f* - the output signal of the FIR1 block, and *r* - the output signal of the FIR2 block. Signals denoted with *o*, *p*, *cf3*, and *cf4*, represent corresponding outputs of all four PDL blocks. Signals with the initial delay are not shown in Fig. 5. Because of this it could be noticed that instead of $+5^o$ phase shift, the phase difference between signals *y* and *o*, is zero, while instead of maximal negative phase shift of -5^o, the phase difference shown here is -10^o.

The circuit was verified for several different phase shift control words. Five of them are selected for representing the verification of the system logic. The first control word is 01111111, which corresponds to the maximal delay of -5^o, which is shown in Fig. 5. The second word is 00001100, for the delay of -2.8425^o. The third control word is 00000000, where no phase shift occurs. Fourth word is 10100100 with positive phase shift of $+2.63^o$. Finally, last control word is 11111111, for the phase shift of $+5^o$.

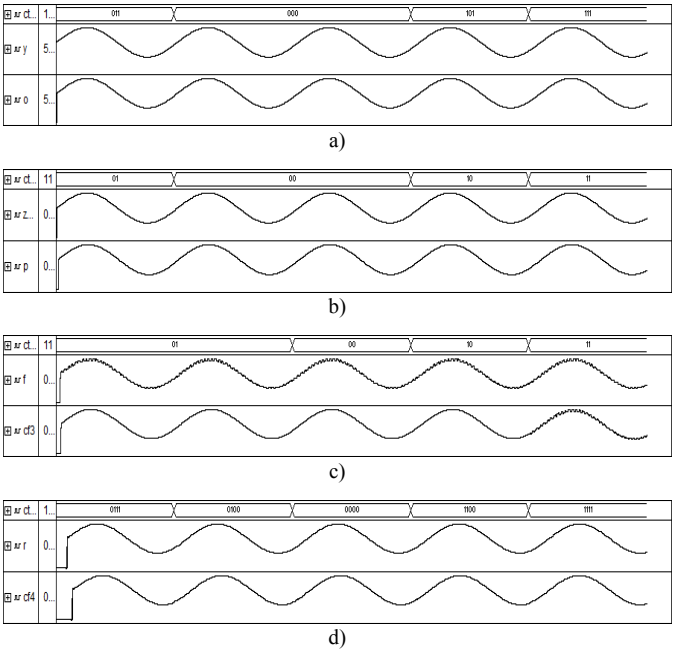

Fig. 5. Illustration of simulation a) programmable delay of the first PDL at 256kHz; b) programmable delay of the second PDL at 64kHz; c) programmable delay of the third PDL at 32kHz; d) programmable delay of the fourth PDL at 16kHz.

All possible programmable values of the phase shift can be decoded according to Tables I-IV. The format of the suitable control word is shown in Fig. 6.

Because of the real values for clock signals, there is a slight mismatch between the calculated and simulated phase shifts. Though, instead of ideally calculated values for phase shift of: $\pm0.25^o$, $\pm0.25^o$, $\pm0.5^o$, and $\pm4^o$, phase shift values of: $\pm0.21^o$, $\pm0.28^o$, $\pm0.5625^o$, and $\pm3.99^o$ respectively are achieved with the described hardware.

Sign bit	ctrl of PDL for 256kHz		ctrl of PDL for 64kHz	ctrl of PDL for 32kHz	ctrl of PDL for 16kHz		
7	6	5	4	3	2	1	0

Fig. 6. Phase shift control word format

At the end, it should be emphasized that the synthesis part of the design will be done after consolidation of two VHDL descriptions that are, decimation line and a PDL line using a suitable Cadence tool for digital synthesis. Also a suitable technology will be chosen.

TABLE I
Decoding table for 16kHz PDL

CTRL(7) & (2 downto 0)				Ph. sh
0	0	0	0	0
0	0	0	1	$0,57^o$
0	0	1	0	$1,14^o$
0	0	1	1	$1,71^o$
0	1	0	0	$2,28^o$
0	1	0	1	$2,85^o$
0	1	1	0	$3,42^o$
0	1	1	1	$3,99^o$
1	0	0	0	0
1	0	0	1	$-0,57^o$
1	0	1	0	$-1,14^o$
1	0	1	1	$-1,71^o$
1	1	0	0	$-2,28^o$
1	1	0	1	$-2,85^o$
1	1	1	0	$-3,42^o$
1	1	1	1	$-3,99^o$

TABLE II
Decoding table for 32kHz PDL

CTRL(7) & (3)		Ph. sh
0	0	0
0	1	$0,5625^o$
1	0	0
1	1	$-0,5625^o$

TABLE III
Decoding table for 64kHz PDL

CTRL(7) & (4)		Ph. sh
0	0	0
0	1	$0,28^o$
1	0	0
1	1	$-0,28^o$

TABLE IV
DECODING TABLE FOR 256KHZ PDL

CTRL(7) & (6 downto 5)			Ph. sh
0	0	0	0
0	0	1	0,07°
0	1	0	0,14°
0	1	1	0,21°
1	0	0	0
1	0	1	-0,07°
1	1	0	-0,14°
1	1	1	-0,21°

VI. CONCLUSION

Digital decimation filters can include some functionality that is not related to filtering. They can provide the fine phase trimming option, which is the functionality that uses already obtained signals from different parts of the decimation line. A procedure for the efficient implementation of programmable delay line in a decimation filter has been presented in this paper. The VHDL description was written for each block in the PDL chain. These blocks were connected and such a description verified by multiple VHDL simulations. The simulations proved the correct functioning of the phase delay line.

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